REMARKS

Reconsideration of this application is respectfully requested in view of the foregoing amendment and the following remarks.

By the foregoing amendment, claims 1, 4, 6-10, 12, 13, 15, 16 and 19 have been amended and claims 3, 5, 14 and 18 have been canceled without prejudice or disclaimer for filing in a continuation application. Thus, claims 1, 4, 6-13, 15-17, 19, 20 and 23-28 are currently pending in the application and subject to examination.

Claims 1, 3-20 and 23-28 Recite Patentable Subject Matter

In the Office Action mailed April 19, 2005, claims 1, 3-20 and 23-28 were rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 6,034,563 to Mashiko. It is noted that claims 3, 5, 14 and 18 have been canceled, and claims 1, 4, 6-10, 12, 13, 15, 16 and 19 have been amended. To the extent that the rejection remains applicable to the claims currently pending, the Applicant hereby traverses the rejection, as follows.

Applicant respectfully submits that each of claims 1, 4, 6-13, 15-17, 19, 20 and 23-28 recites subject matter that is neither disclosed nor suggested by the applied art of record.

Independent claims 1, 8, 9 and 13 recite, in part:

> a waveshaping circuit which receives a control signal...and performs waveshaping so that an output signal of said waveshaping circuit rises slower than said control signal...

The outstanding Office Action asserts that the waveshaping circuit of the claimed invention reads on either circuit 15 or the combination of circuits 13 and 15 of Mashiko. Applicant respectfully submits that in Fig. 3, Mashiko discloses that the rise time of a

control signal S1 and a voltage VPP, which are input to the selecting circuit 15, a voltage VDD, which is input to the high voltage generating circuit 13, and a control signal SL, which is output from the selecting circuit 15, all have a same rise time. Thus, Applicant submits that Mashiko neither discloses nor suggests at least the feature of a waveshaping circuit which receives a control signal...and performs waveshaping so that an output signal of said waveshaping circuit rises slower than said control signal, as recited in claims 1, 8, 9 and 13.

Claims 1, 8 and 9 further recite, in part:

> said waveshaping circuit comprises a high-threshold final-stage MIS field effect transistor, or a plurality of high-threshold final-stage MIS field effect transistors connected in series.

The Office Action asserts that the waveshaping circuit of claims 1, 8 and 9 reads on either circuit 15 or the combination of circuits 13 and 15 of Mashiko. Applicant respectfully submits that neither the high voltage generating circuit 13 nor the selecting circuit 15 of Mashiko has a high-threshold final-stage MIS field effect transistor, or a plurality of high-threshold final-stage MIS field effect transistors connected in series, as does the waveshaping circuit recited in claims 1, 8 and 9. Rather, as disclosed at col. 1, lines 62-67, col. 7, line 48 - col. 8, line 28, and in Fig. 2 of Mashiko, the transistors of circuits 13 and 15 are not high threshold transistors (i.e., they have threshold voltages ~ .2 to .3 V, lower than VDD). Thus, Mashiko fails to disclose or suggest at least the feature of a waveshaping circuit comprising a high-threshold final-stage MIS field effect transistor, or a plurality of high-threshold final-stage MIS field effect transistors connected in series, as recited in claims 1, 8 and 9.

Claims 9 and 13 further recite, in part:

> a level conversion circuit which receives a control signal of a first level...and which converts said control signal of said first level into a control signal of a second level and supplies said control signal of said second level...

The outstanding Office Action asserts that the level conversion circuit of claim 9 "reads on circuit 13, and the recited first and second control signal levels are the levels of S1 and SL." *See the Office Actions of April 19, 2005 at p. 2, December 1, 2004, at p. 3 and July 12, 2004, at p. 3.*

Applicant respectfully submits that circuit 13 of Mashiko is a high voltage generating circuit, which receives as an input high voltage supply VDD and outputs a voltage VPP to the selecting circuit 15. The high voltage generating circuit 13 of Mashiko neither receives the control signal S1, nor does the high voltage generating circuit 13 output the control signal SL. Thus, Applicant respectfully submits that Mashiko neither discloses nor suggests a level conversion circuit which receives a control signal of a first level...and which converts said control signal of said first level into a control signal of a second level and supplies said control signal of said second level to a gate of said high-threshold N-channel type (claim 9) or P-channel type (claim 13) MIS field effect transistor, as recited in claims 9 and 13.

To establish prima facie obviousness of a rejected claim, the applied art of record must teach or suggest each feature of a rejected claim. *See M.P.E.P. §2143.03 and In re Rouffet, 149 F.3d 1350, 1357, 47 USPQ2d 1453, 1457-58 (Fed. Cir. 1998).* As explained above, Mashiko neither discloses nor suggests each and every feature recited in independent claims 1, 8, 9 and 13. Therefore, independent claims 1, 8, 9 and

13, are neither anticipated nor rendered obvious by Mashiko. Accordingly, Applicant respectfully submits that independent claims 1, 8, 9 and 13 are patentably distinct over Mashiko and in condition for allowance.

Claims 4, 6, 7, 23 and 24 depend from claim 1, claims 25 and 26 depend from claim 8, and claims 10-12, 15-17, 19, 20, 27 and 28 depend from claim 9. Thus, claims 4, 6, 7, 10-12, 15-17, 19, 20 and 23-28 are allowable for at least the same reasons as claims 1, 8, and 9, as well as for the additional subject matter recited therein.

Applicant respectfully requests withdrawal of the rejection of claims 1, 4, 6-13, 15-17, 19, 20 and 23-28 under 35 U.S.C. § 103(a).

Conclusion

For all of the above reasons, it is respectfully submitted that claims 1, 4, 6-13, 15-17, 19, 20 and 23-28 are in condition for allowance and a Notice of Allowability is earnestly solicited.

Should the Examiner determine that any further action is necessary to place this application into better form, the Examiner is invited to contact the undersigned representative at the telephone number listed below.

In the event this paper is not considered to be timely filed, the Applicant hereby petitions for an appropriate extension of time. The Commissioner is hereby authorized to charge any fee deficiency or credit any overpayment associated with this communication to Deposit Account No. 01-2300 referencing client matter number 100021-00133.

Respectfully submitted,

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